REMARKS

Claim Rejections Under U.S.C. § 112

Claims 1-4 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1-4, Applicant has amended claims 1 and 4 to clarify what is claimed. As claims 2-3 depend from the independent claim 1, they are also considered to be allowable. The Applicant therefore respectfully requests that the rejection of claims 1-4 under 35 U.S.C. § 112, second paragraph be withdrawn.

Additional Claim Amendments

Applicant has also amended claim 15 outside of any current rejection to correct a typographical error by the deletion of "wherein the 5". The Applicant submits that the amendment adds no new matter and that, as detailed below, claim 15 to be in condition for allowance. Accordingly, Applicant respectfully requests the consideration and allowance of claim 15 as amended.

Claim Rejections Under U.S.C. § 102

Claims 1, 3 and 14-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Motoshima et al., Patent No. 5,847,994.

Applicant respectfully traverses this rejection and feels that claims 1, 3 and 14-19, as amended, are allowable for the following reasons.

The Examiner stated that "[w]ith regard to claim 1, as far as understood Motoshima discloses a flash memory device comprising: a memory array (fig.2, BLK0-BLKn) having erasable blocks of memory cells, each block of memory cells being arranged in a row and column configuration, wherein each column of memory cells is couplable to an associated bit line (fig.2, WBL0, RBL0 . . . WBL1-RBL1); control circuitry (fig. 1, 9) to control memory operations to the

memory array; a verify sense amplifier (fig2, 12) to verify a program state of the memory cells, the verify sense amplifier is coupled to a first location of the bit lines (fig. 2, a node between WBL0 and verifying sense amplifier 12); a read sense amplifier (fig. 2, 10) to read a program state of the memory cells, the read sense amplifier is coupled to a second location of the bit lines (fig. 2, a node between RBL0 and read sense amplifier 10); and a switch (fig. 2, WYG0, RYG0, WYG1, RYG1) to selectively couple either the verify sense amplifier or the read sense amplifier to an output circuit."

Applicant respectfully disagrees and maintains that Motoshima, et al. teaches a non-volatile memory device that has two separate sets of read (RBL) and write (WBL) bit lines that are separately couplable to the memory cells and allow separate read and write operations to occur at the same time on the same memory array in a background operation (BGO) mode. The read bit lines (RBL0, RBL1) are selectively coupled to the read sense amplifier 10 through the read Y-gates (RYG0 and RYG1) and the write bit lines (WBL0, WBL1) are selectively coupled through the write Y-gates (WYG0 and WYG1) to the verify sense amplifier 12. *See, e.g.*, Motoshima, et al., column 6, lines 3-19, column 7, line 64 to column 8, line 55, column 2, line 64 to column 3, line 36, Figure 2 and Figure 10.

As such, Applicant submits that Motoshima, et al. fails to teach a non-volatile memory device with a memory array having erasable blocks of memory cells, each block of memory cells being arranged in a row and column configuration, wherein each column of memory cells is couplable to an associated bit line, a verify sense amplifier coupled to the associated bit lines, and a read sense amplifier coupled to the associated bit lines.

Applicant's claim 1 is directed to a flash memory device comprising a memory array having erasable blocks of memory cells, each block of memory cells being arranged in a row and column configuration, wherein each column of memory cells is couplable to an associated bit line; control circuitry to control memory operations to the memory array; a verify sense amplifier to verify a program state of the memory cells, the verify sense amplifier is coupled to the associated bit lines; a read sense amplifier to read a program state of the memory cells, the read sense amplifier is coupled to the associated bit lines; and a switch to selectively couple either the verify sense amplifier or the read sense amplifier to an output circuit. As detailed above,

Applicant submits that Motoshima, et al. fails to teach such a flash memory device having a memory array having erasable blocks of memory cells, each block of memory cells being arranged in a row and column configuration, wherein each column of memory cells is couplable to an associated bit line, a verify sense amplifier coupled to the associated bit lines, and a read sense amplifier coupled to the associated bit lines.

Regarding claim 3, as it depends from and further defines patentably distinct claim 1 it is also considered to be in condition for allowance.

In addition, Applicant respectfully disagrees with the Examiner's argument that Motoshima, et al. discloses that the verify sense amplifier and the read sense amplifier have an inherent adjustable sensitivity. Applicant can find no mention of the verify sense amplifier or read sense amplifier having an adjustable sensitivity in Motoshima, et al. to support the Examiner's assertion and respectfully requests that such be given. If the Examiner is relying on the verify and read sense amplifiers being inherently adjustable, the Applicant requests that the Examiner state the rational or evidence supporting this assertion as the Examiner is required to do in MPEP §2112. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). *See*, MPEP §2112.

Regarding claim 14, Applicant respectfully disagrees with the Examiner's argument that claims 14-19 encompass the same scope of invention as claims 1 and 3 and thus stands rejected for the same reasons as claims 1 and 3. Claim 1 is directed towards a flash memory device comprising a memory array having erasable blocks of memory cells, each block of memory cells being arranged in a row and column configuration, wherein each column of memory cells is couplable to an associated bit line, a verify sense amplifier coupled to the associated bit lines, and a read sense amplifier coupled to the associated bit lines. Applicant's claim 14 is directed to a method of calibrating a non-volatile memory comprising reading a data state of a plurality of memory cells with a first sense amplifier; reading the data state of the plurality of memory cells with a second sense amplifier; comparing outputs of the first and second sense amplifiers to

determine offsets between the first and second sense amplifiers; and adjusting either the first or second sense amplifier to calibrate the first and second sense amplifiers. As such, Applicant submits that claims 1 and 14 are inherently of differing scope.

In addition, Applicant submits that Motoshima, et al. does not teach or disclose a method or apparatus for calibrating a non-volatile memory, wherein a plurality of memory cells are read with a first and second sense amplifiers, the outputs of the first and second sense amplifiers compared to determine offsets, and adjusting either the first or second sense amplifiers.

Applicant respectfully contends that claims 1 and 14 as pending have been shown to be patentably distinct from the cited reference. As claims 3 and 15-20 depend from and further define claims 1 and 14 they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 3 and 14-20.

Claim Rejections Under U.S.C. § 103

Claims 2 and 4 were rejected under 35 U.S.C. § 103(a) as being anticipated by Motoshima et al., Patent No. 5,847,994.

Applicant respectfully traverses this rejection and feels that claims 2 and 4, as amended, are allowable for the following reasons.

Applicant respectfully disagrees and believes that there are significant differences in the reference, and that the disclosed invention would not be apparent to one skilled in the art.

As stated above in regards to the rejection of independent claim 1, which claims 2 and 4 depend from, Motoshima, et al. fails to teach a non-volatile memory device with a memory array having erasable blocks of memory cells, each block of memory cells being arranged in a row and column configuration, wherein each column of memory cells is couplable to an associated bit line, a verify sense amplifier coupled to the associated bit lines, and a read sense amplifier coupled to the associated bit lines. As such, Motoshima, et al. fails to teach or disclose independent claim 1 and therefore does not teach or disclose all elements of claims 2 and 4.

Furthermore, regarding claim 4, Applicant maintains that as Flash memory devices reuse the read sense amplifier to verify write data and that most integrated circuits utilize a uniform process size, that it would not be apparent to one skilled in the art to reduce the feature size of transistors a read sense amplifier to a size lower than that required by the write operating voltage.

Applicant respectfully contends that claims 2 and 4 as pending have been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 2 and 4.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that all claims are in condition for allowance and requests reconsideration of the application and allowance of claims.

The Examiner is invited to contact Applicant's attorney to discuss any questions that may remain with respect to the present application.

Respectfully submitted,

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Date 7/9/03

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